

Application No. 09/996,681

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**LISTING OF CLAIMS:**

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Cancelled)

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10. (Original) A method for dicing die from a semiconductor wafer while allowing a very close cut of a die edge relative to active elements on the die without damaging the active elements comprising:

etching by way of a first dry etch an opening down to the surface of the semiconductor wafer;

etching by way of a second dry etch a U-groove in the opening down to the surface of the semiconductor wafer created by the first dry etch; and

sawing the semiconductor wafer along the U-groove where one edge of the saw is substantially in alignment with the bottom of the U-groove.

11. (Original) The method of claim 10 wherein the first dry etch comprises SF<sub>6</sub> as the main active gas component.

12. (Original) The method of claim 10 wherein the second dry etch uses a combination of gases comprising SF<sub>6</sub> and O<sub>2</sub>.

13. (Original) The method of claim 10 wherein the opening at the surface is 3.5 to 5.5 microns wide.

14. (Original) The method of claim 10 wherein the U-groove is approximately 4 microns in depth.

15. (Original) The method of claim 10 wherein the U-groove is approximately 3.5 to 5.5 microns in depth.

16. (Original) The method of claim 10 wherein the U-groove is approximately 6 to 10 microns in width.

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17. (Original) The method of claim 10 wherein the semiconductor wafer is comprised of amorphous silicon.

18. (Original) The method of claim 10 wherein the semiconductor wafer is comprised of a III-V compound.

19. (Original) The method of claim 10 wherein the semiconductor wafer is comprised of gallium arsenide.

20. (Original) The method of claim 10 wherein the semiconductor wafer is comprised of silicon on insulator.

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21. (Previously Presented) A method of fabricating high resolution image sensor dies from a wafer so that the dies have precision faces to enable the dies to be assembled with other like dies to form a larger array without image loss or distortion at the points where the dies are assembled together, comprising the steps of:

etching by way of a first dry etch an opening down to the surface of the semiconductor wafer;

etching by way of a second dry etch small U-shaped grooves in the opening down to the surface of the semiconductor wafer created by the first dry etch;

forming grooves in the opposite side of the wafer opposite each of the U-shaped grooves, the axis of the grooves being parallel to the axis of the U-shaped groove opposite thereto; and

sawing the wafer along the U-shaped grooves with one side of the cut made by sawing being substantially coextensive with the bottom of the U-shaped grooves whereby one side of the U-shaped grooves is at least partially obliterated by the sawing, the sides of the U-shaped grooves that remain serving to prevent development of fractures in the die beyond the remaining side as the wafer is being sawed.

22. (Original) The method of claim 21 wherein the etching is a dry etch using a combination of gases comprising SF<sub>6</sub> and O<sub>2</sub>.

23. (Original) The method of claim 22 wherein the opening at the surface is 3.5 to 5.5 microns wide.

24. (Original) The method of claim 22 wherein the U-groove is approximately 4 microns in depth.

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25. (Original) The method of claim 22 wherein the U-groove is approximately 3.5 to 5.5 microns in depth.

26. (Original) The method of claim 22 wherein the U-groove is approximately 6 to 10 microns in width.